

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-11685 US		09/905,474	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)			
(Use several sheets if necessary)				Seputro, Stephanus D.; Zhang, Lan			
				Filing Date		Group	
				July 13, 2001		2827	
U.S. Patent Documents							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
Foreign Patent Documents							
						Translation	
	Document	Date	Country	Class	Subclass	Yes	No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ	David A. Baranuskas and Douglas E. Wallace, Jr., "Capacitive Structure for Via Impedance Tuning"; September 14, 1999, Serial No. 09/395,788. 361/793 Am 204T2827					
	AR	Doreen S. Fisher and Thad McMillian, "Printed Circuit Assembly Having Conductive Pad Array With In-Line Via Placement", June 28, 2000, Serial No. 09/605,905. 361/777 Am 254T2827					
	AS						
Examiner	John B. Vignone		Date Considered June 29, 2003				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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